## REMARKS

Favorable reconsideration of this application as presently amended and in light of the following discussion is respectfully requested.

Claims 1, 2, 4, 6, 7, 9-11, and 13-15 are presently active in this case, Claims 1 and 10 having been amended and Claims 3, 5, 8, and 12 having been canceled without prejudice or disclaimer by way of the present Amendment. Care has been taken such that no new matter has been entered.

In the outstanding Official Action, Claims 1-15 were rejected under 35 U.S.C. 103(a) as obvious of Gerber et al. (U.S. Patent No. 5,401,913) in view of either one of Bohn (U.S. Patent No. 6,537,412) or Johnston (U.S. Patent No. 5,153,050) and Endomoto et al. (WO 98/56220). For the reasons discussed below, the Applicant requests the withdrawal of the obviousness rejections.

The basic requirements for establishing a *prima facie* case of obviousness as set forth in MPEP 2143 include (1) there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or to combine reference teachings, (2) there must be a reasonable expectation of success, and (3) the reference (or references when combined) must teach or suggest all of the claim limitations. The Applicant submits that a *prima facie* case of obviousness cannot be established in the present case because the references, either taken singularly or in combination, do not teach or suggest all of the claim limitations.

Claim 1 of the present application recites a method of manufacturing a multilayer

circuit board that includes a insulating substrate comprising a one-side copper-clad laminate wherein a plated conductor is formed in a via hole therethrough so that the entire plated conductor is recessed from a surface of the insulating substrate, and a conductive bump having a rounded end is formed on the plated conductor so that the conductive bump projects from the surface of the insulating substrate. The method includes stacking the printed board in a manner set forth in the claim and integrating an outermost conductor layer, the printed board with the conductor circuit, and a second printed board by one time of pressing such that the conductive bump in each printed circuit board pierces through an adhesive therebetween and is connected to the conductor circuit or the copper foil, and thereafter, etching the copper foils on opposite surfaces, thereby obtaining the multilayer circuit board.

Claim 10 recites a method of manufacturing a multilayer circuit board, in which a plurality of printed boards are stacked and pressed into a multilayer circuit board. In the method, a plated conductor fills a via hole with an amount determined so that the entire plated conductor is recessed from the surface of the insulating substrate, and the plated conductor is formed with a conductive bump having a rounded end that projects from the surface of the insulating substrate and extends through the bonding layer so that the conductive bump is connected to the conductor layer of another stacked printed board. The method also includes pressing a stack so that the printed boards and the outermost conductor layer are bonded together such that the conductive bump in each printed board pierces through an adhesive therebetween and is connected to the conductor circuit or the copper foil.

In the above methods recited in Claims 1 and 10, a plated conductor is formed in a via hole such that the entire plated conductor is recessed from the surface of the insulating

substrate, and the plated conductor is formed with a conductive bump having a rounded end that projects from the surface of the insulating substrate. Additionally, the printed boards described therein are stacked and pressed such that the conductive bump in each printed circuit board pierces through an adhesive therebetween and is connected to the conductor circuit or the copper foil. As will be discussed below, the cited references, either taken singularly or in combination, fail to disclose or suggest such methods.

The Official Action cites the Gerber et al. reference for the teaching of a plated conductor formed in a via hole. However, the Applicant submits that the Gerber et al. reference does not disclose a plated conductor that is formed in a via hole such that the entire plated conductor is recessed from the surface of the insulating substrate as recited in amended Claim 1, or a plated conductor that fills a via hole with an amount determined so that the entire plated conductor is recessed from the surface of the insulating substrate as recited in Claim 10. The Official Action cites feature (20) in the Gerber et al. reference for the teaching of the plated conductor of the present invention, however, as is clearly evident from the figures of the Gerber et al. reference, a portion of feature (20) extends above the surface of the layer (10).

In fact, the Applicant submits that the teaching of feature (20) in the Gerber et al. reference could not be modified to include an entire plated conductor that is recessed from the surface of the insulating substrate as recited in the present application, since such a configuration would be contrary to the teachings of feature (20) set forth in the Gerber et al. and therefore no motivation would have existed to make such a combination or modification.

More specifically, the Gerber et al. reference teaches that feature (20) is constructed such that it includes a bump or crown "that extends above the top surface of circuit board 10" in order to electrically interconnect adjacent circuit board layers. (See column 4, line 68, through column 5, line 5.) Thus, the modification of feature (20) such that the entirety thereof is recessed below layer (10) (e.g., through the combination with another reference) would be contrary to the teachings of the Gerber et al. reference, and thus no motivation would exist to make such a modification absent the improper use of hindsight considerations. Thus, not only does the Gerber et al. reference not teach this limitation from Claims 1 and 10 of the present application, but also the Gerber et al. reference is not combinable with a reference that teaches such a feature since such a combination would be contrary to the teachings of the Gerber et al. reference.

Accordingly, the Applicant respectfully submits that a *prima facie* case of obviousness cannot be established with respect to Claims 1 and 10 of the present application. Thus, the Applicant respectfully requests the withdrawal of the obviousness rejections of Claims 1 and 10.

The dependent claims are considered allowable for the reasons advanced for the independent claim from which they respectively depend. These claims are further considered allowable as they recite other features of the invention that are neither disclosed nor suggested by the applied references when those features are considered within the context of their respective independent claim.

Consequently, in view of the above discussion, it is respectfully submitted that the present application is in condition for formal allowance and an early and favorable reconsideration of this application is therefore requested.

Respectfully Submitted,

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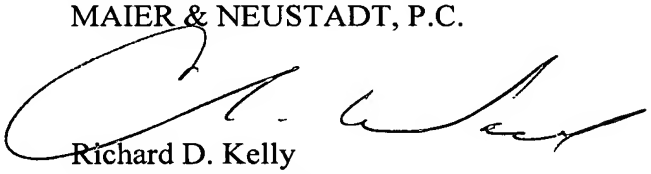

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